1. **Title of the document**

Performance Analysis of Tunnel Field-Effect Transistors

1. **Identification**

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1. **Abstract**

For over five decades, the miniaturization of circuits, achieved by the scaling down of metal-oxide field- effect transistors (MOSFETs), has been the principal driver for the semiconductor industry. However, the stringent power constraints of integrated circuits and the non-scalability of the subthreshold slope in a conventional MOSFET, now pose a serious threat to the continued scaling of the field-effect transistor. Therefore, intensive research is being carried out on novel steep subthreshold-slope devices the conventional MOSFET can replace that in future integrated circuits. Hence, Tunnel Field Effect Transistors (TFETs) are very promising devices as they exhibit a subthreshold swing lower than 60Mv/decade, which is the theoretical limit for a conventional MOSFET. TFET-based circuits can be energy efficient.

It triggered an exhaustive research of TFETs around 2004 with the successful demonstration of the subthreshold swing below 60mV/decade and the necessity for a device that can replace conventional MOSFETs for low-power energy-efficient circuits. Since then there has been a thorough investigation of various aspects of TFETs and their applications in integrated circuits. The number of research papers on TFETs has been growing.

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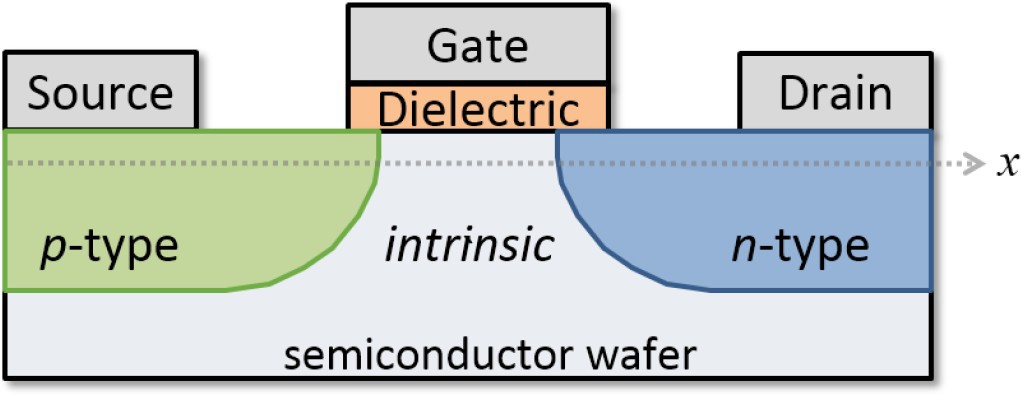
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# Introduction

As it scales MOSFETs down, the power supply voltage should also go down to reduce power density. For example, a 45-nm low-operating-power device should have a power supply voltage of 0.9 V. To maintain a high ON-state current with an acceptable OFF-state leakage, a reduction of the subthreshold swing (SS) is necessary and has emerged as one of the most important technological issues. However, even in the ideal case of inﬁnite gate capacitance, the SS of MOSFETs cannot be reduced below 60 mV/dec at room temperature. They have proposed some novel devices to achieve a sub-60- mV/dec SS such as impact-ionization MOS devices, nanoelectromechanical FETs, suspended gate MOSFETs

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and tunneling FETs (TFETs). Among them, this report focuses on the TFET. The TFET is a gated P-N diode operating under reverse bias, Unlike the MOSFET which uses thermal carrier injection, the TFET uses the band-to-band tunneling as a source carrier injection mechanism.

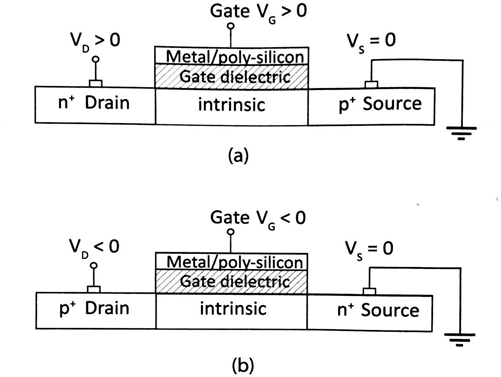


# FIGURE 1

Basic TFET structure [1].

# Methodology

DEVICE STRUCTURE



# FIGURE 2

A simple implementation of a TFET and the biasing scheme: (a) n-type TFET

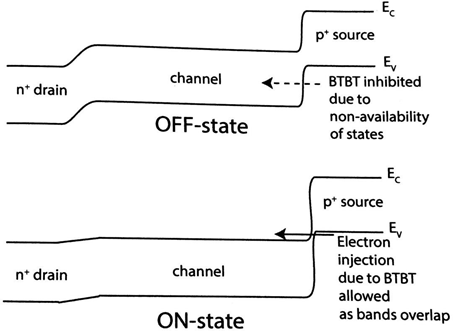
1. P-type TFET [1].

In simple terms, the TFET is a gated reverse bias p-in structure. It shows a simple implementation of an n-type and p-type TFET in above figure. the most distinguishing feature of a TFET is the doping of the drain and the source. The doping of the drain and the source are of opposite types in a TFET. In contrast, the drain and the source doping are of the same type in a conventional MOSFET. For an n-type of TFET, it dope the drain n+ while it dope the source p+. For a p-type TFET, it dope the drain p+ while it dope the source n+. The channel is an intrinsic or doped p-type or n-type

Semiconductor. It separates the channel from the gate electrode by a dielectric, similar to a conventional MOSFET.

It shows the biasing schemes of an n-type and a p-type TFET in the figure. For an n-type TFET, the source is grounded and a positive voltage applies to the drain and the gate electrodes. For p-type TFET, the source is grounded and a negative voltage applies to the drain and the gate electrodes. They call a TFET an n-type TFET or a p-type TFET depending on the dominant carrier in the channel formed under the gate when the TFET is turned on. When the dominant carriers in the channel are electrons, they call the TFET an n-type TFET and when the dominant carriers in the channels are holes; they call the TFET p-type TFET. They call the terminals source or drain depending on whether the dominant carriers enter or leave the channel through that terminal. The mechanism of the dominant carriers entering the channel is band-to-band tunneling (BTBT).

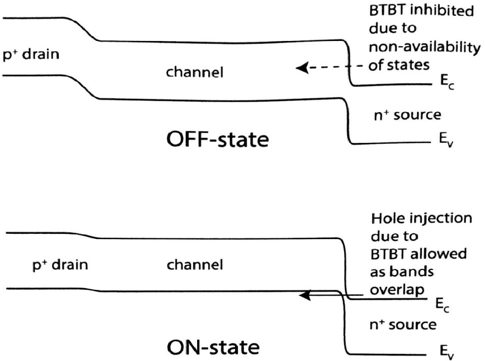
DEVICE OPERATION



**FIGURE 3**: Band diagram of an n-type TFET in the OFF-state and in the ON-state [1].

They base the operation of a TFET on band-to-band tunneling (BTBT). BTBT involves tunneling of carriers from the valence band into the conduction band through the forbidden band gap or vice versa.

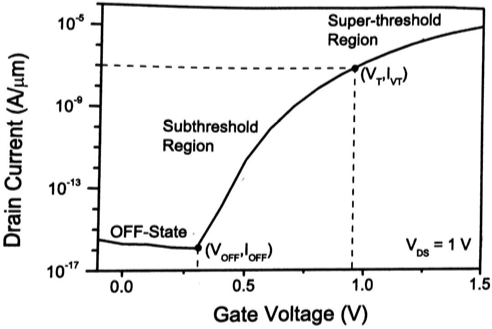
It shows Band diagrams of an n-type TFET in the figure in the OFF-state and in the ON–state. When the gate voltage is close to zero, the TFET is in the OFF- state. The conduction band in the channel lies above the valence band in the source. As a result, it inhibits BTBT, and the TFET is in the OFF-state with low drain current. When the gate voltage is increased, the gate voltage modulates the carrier density below the gate and the conduction band in the channel pushed down. When a high voltage applies to the gate, there is band bending at the source such that the valence band in the source and the conduction band in the channel get aligned, as shown in the figure. As a result, the electrons in the valence band in the source can tunnel to the conduction band in the channel. It sweeps the electrons that tunnel into the channel to the drain terminal by the positive bias of the drain. This forms the basis of operation for an n-type TFET.



**FIGURE 4:** Band diagram of a p-type TFET in the OFF-state and in the ON-state [1].

It shows the band diagrams of a p-type TFET the figure in the OFF-state and in the ON-state. The principle of operation of a p-type TFET is like the n-type TFET. When the gate voltage is close to zero, the TFET is in the OFF- state. When a large negative voltage applies to the gate, they push the valence band in the channel above the conduction band in the source as shown in the figure. As a result, they inject holes into the channel which is swept to the drain terminal by the negative bias of the drain. This forms the basis of operation for a p-type TFET.

TRANSFER CHARACTERISTICS OF TFET



**FIGURE 5:** Simulated transfer characteristics of the TFET at VDS= 1V [9].

The figure shows the simulated transfer characteristics of the TFET at VDS= 1 V, got by sweeping the gate voltage from VGS= -0.1 V to VGS = 1.5 V. We can divide the transfer characteristics of a TFET into three regions:

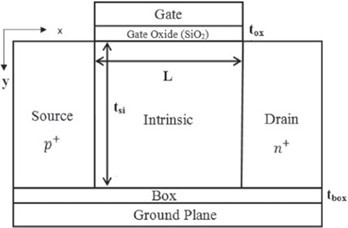
* 1. OFF-state (0 < VGS < VOFF): In this region the TFET has a low current and BTBT is inhibited. VOFF is the gate voltage at which the drain current takes off.
  2. Subthreshold region (VOFF < VGS < VT): In this region the drain current rises. VT is the threshold voltage of the TFET.
  3. Super-threshold region (VGS < VT): In this region, the drain current rises with the gate voltage at a reduced rate.

DIFFERENT TYPES OF TFETs

TFETs have been proposed and realized in various structural forms. Based on the gate structure in the TFET, they can classify the TFETs as single- gate TFET, double-gate TFET, or gate-all-around TFET. The double-gate- TFET and gate-all-around TFET have better control over the channel potential compared to a single-gate TFET. They have realized test with a homojunction at the source and a heterojunction at the source. The heterojunction TFET achieves a much lower effective bandgap than a homojunction TFET [3]. Different semiconducting materials like silicon, Germanium, Carbon and III-V semiconductor materials have been incorporated into the TFETs. Materials like nanowires, CNTs, and graphene that exhibit quantum confinement effects are also being investigated for TFETs. These material have special properties they can exploit that to improve the electrical characteristics of the TFETs.

# Results & Discussions

IMPACT OF DEVICE PARAMETERS



**FIGURE 6:** Silicon on insulator tunnel field-effect transistor [2].

# GATE DIELECTRIC

They expect the drain current to increase with an increase in the dielectric constant of the gate material or decrease in gate dielectric thickness. It has been analyzed an verified that the tighter gate control got by using a high-*k* dielectric material or decreasing the gate dielectric thickness results in increasing the ION of the TFET.

# BODY THICKNESS

The impact of the silicon body thickness on the drain current depends on two competing effects

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As the silicon body thickness increases, the volume of silicon available for BTBT increases, increasing the drain current. However, as the thickness of the silicon body increases, the coupling of the gate with the channel degrades, leading to a decrease in drain current.

# SOURCE DOPING CONCENTRATION AND PROFILE

When the source doping concentration is increased, the band gap narrowing increases, which results in a decrease in the tunneling distance. For high source doping concentration, due to the changed built-in potential at the source- channel junction, the threshold voltage is expected to reduce. The tunneling current also depends on the abruptness of the source doping profile. With the increase in the abruptness of the source doping, the electric field at the source-channel junction increases, resulting in an increase in the tunneling current.

# CHANNEL LENGTH

The tunneling current depends on the electric fields and the band alignment near the source-channel junction, the tunneling current does not change much with the decrease on the channel length.

AMBIPOLAR CURRENT

There are two tunneling junctions in TFET: the source-channel tunneling junction and the drain-channel tunneling junction. the BTBT in the drain channel junction is suppressed in a TFET by reducing the drain doping or using other technique. However, when the TFET is symmetric, i.e., the same doping concentration but of opposite type is used on the source side and on the drain side, then the TFET exhibits am bipolar behavior. Am bipolar behavior means that the same TFET shows n-type behavior with the electrons contributing majorly in current transport and a p-type behavior with the holes contributing majorly in the current transport, at the same drain voltage VD. An n-type TFET can conduct for the positive VG with BTBT on the source side and for the negative VG with BTBT on the drain side, keeping the VD positive., a p-type TFET can conduct for the negative VG with BTBT on the source side and for the positive VG with BTBT on the drain side, keeping the VD negative.

MINIMIZATION OF AMBIPOLAR CURRENT

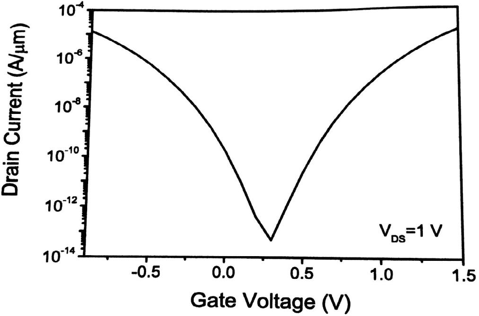
1. Reducing drain doping.
2. Creating a drain-gate underlap.
3. Using a heterojunction.
4. Introducing some kind of asymmetry into the TFET structure
5. 
6. **FIGURE 7:** Transfer Characteristics of the DGTFET with the same doping on the source and the drain [9].

Figure the transfer characteristics of a TFET that has the same doping concentration for the source and the drain. When VG is positive, the conduction band and valence band get aligned on the source side, as in the normal n-type mode of operation of TFET. However, when VG is negative, the bands get aligned on the drain side, resulting BTBT on the drain side.

TEMPERATURE DEPENDENCE OF TUNNELING FETS

They investigate the temperature and voltage dependence of the GIDL effect in MOSFETs under low electric field. They can express the dependency of the GIDL current on the electric field as

IGIDL α AE5/2 expr (-B/E)

The parameter is given by A ∝ they derive E -7/4 Gand B ∝ E 3/2, to be very weak dependence on the temperature. However, a second effect exists at a low electric field. Under low electric field, the Shockley-Read-Hall (SRH) model, which has a strong temperature dependence can describe the GIDL current. Under, higher electric field the GIDL current is dominated by Band-to-Band tunneling which has a weak temperature dependence. Due to the comparable physical principle of the GIDL current and the TFET, Eqn. can separate the SRH part of the TFET characteristic from the Band-to-Band tunneling part. Hence, starting from a gate-to-source voltage of 1V the Band-to-Band tunneling is the dominant mechanism. Like for the MOSFET the temperature dependency is changing with the voltage applied. For the MOSFET they can use the zero temperature coefficient point for digital circuit design to make the system performance independent of the temperature. For, the TFET the voltage where the change of the temperature dependence occurs is outside the usable range. Hence, the combination of the MOSFET and the TFET can compensate for temperature effects. For analog circuits, the temperature dependence has to be verified in more detail. the temperature effect of the TFET is more comparable to the bipolar device [10].

APPLICATIONS OF TFET

TFET or tunnel FETS are similar to MOSFETs and applications of these two are similar to a digital switch, etc. The working principle of TFETs differs greatly from MOSFETs. In MOSFETs, the flow of current will be due to diffusion phenomenon, while in Tunnel FETs, it allies the conduction mechanism to Zener Tunneling.

The TFET belongs to the family of so-called steep slope devices that are being examined for ultra-low-power electronic applications, Because of their low-off currents, they are suitable for low-standby-power logic and low-power applications functioning at moderate frequencies. Other applications of tunnel FETS include ultra-low- power specific analog ICs (integrated circuits) with better temperature strength and low-power SRAM.

The main advantages of TFETs include:

* Having Less SS<60 mV/decade.
* Low power requirement.

# Conclusion

TFET is one of the most promising exploratory devices since they exhibit a subthreshold swing lower than 60mv/decade which is a theoretical limit for a conventional MOSFET at room temperature. TFET based circuits can be energy-efficient and they often regard TFETs as “**green transistor**”.

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